REMARKS

Restriction Requirement

The Office Action requires a Restriction to one of two inventions: Group I, claims 1-14 and claims 23-36; and Group II, claims 15-22 under 35 U.S.C. §121. The Applicant herein elects Group 1, claims 1-14 and claims 23-36, with traverse in order to expedite the prosecution of this application. The Applicant intends to prosecute the claims of Group II in a future divisional patent application claiming priority to the present application.

Rejection Under 35 U.S.C. §112

Claims 1-14 and 23-36 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regards as the invention.

Claims 1, 4-5, 34, and 36 were rejected because the term "multiple processors" lacks proper antecedent basis. Claims 1, 5, 34, and 36 have been amended to recite at least one processor in the configurable multiple processor, distributed memory hardware architecture. Claim 4 has been amended to recite at least two processor in the configurable multiple processor, distributed memory hardware architecture. The Applicants submit that these claim amendment overcome this rejection under 35 U.S.C. §112.

Claims 3, 13-14, 34, and 36 were rejected because the term "distributed memories" lacks proper antecedent basis. Claims 3, 13-14, 34, and 36 where amended to recite at least one distributed memory in the configurable multiple processor, distributed memory hardware architecture. The Applicants submit that these claims amendments overcome this rejection under 35 U.S.C. §112.

Claim 6 was rejected because the term "the tasks" lacks proper antecedent basis. Claim 6 was amended to recite the method of claim 1 wherein the predicting the schedule of tasks comprises using a resource-based model of the configurable multiple processor, distributed memory hardware architecture to predict the schedule of tasks. Claim 6 as originally filed included the term "the schedule of tasks." The Applicants submit that the

term "the schedule of tasks" has the proper antecedent basis in the term "predicting a schedule of tasks for the task-level network of behaviors" in independent claim 1 as currently amended. The Applicants submit that claim 6 is not indefinite under 35 U.S.C. §112.

Claims 6 and 35 were rejected because the term "the architecture" lacks proper antecedent basis. Claim 6 was amended to recite "the configurable multiple processor, distributed memory hardware architecture." The Applicants submit that the term "the configurable multiple processor, distributed memory hardware architecture" has the proper antecedent basis in the term "a configurable multiple processor, distributed memory hardware architecture" in independent claim 1 as currently amended. Claim 35 was also amended to recite "the configurable multiple processor, distributed memory hardware architecture." The Applicants submit that the term "the configurable multiple processor, distributed memory hardware architecture" has the proper antecedent basis in the term "a configurable multiple processor, distributed memory hardware architecture" in independent claim 34 as currently amended. The Applicants submit that these claims amendments overcome this rejection under 35 U.S.C. §112.

Claim 29 was rejected because the term "the least negative" lacks proper antecedent basis. Claim 29 was amended to recite "a least negative." The Applicants submit that this claim amendment overcome this rejection under 35 U.S.C. §112.

Claim 35 was rejected because the term "the means for" lacks proper antecedent basis. Claim 35 as originally filed includes the term "further comprising means for producing machine executable code." Claim 35 was amended to recite "further comprising a means for producing machine executable code." The Applicants submit that this claim amendment overcome this rejection under 35 U.S.C. §112.

The Office Action states that the term "mapping a plurality of tasks and data onto a multiple processor, distributed memory hardware architecture" in claim 1 is not clearly understood. Claim 1 has been amended to recite a method of mapping a plurality of tasks and mapping a plurality of data onto a multiple processor. The Office Action also states that it is uncertain what the term "a task-level network of behaviors" refers to in claim 1. Claim 1 has been amended to recite the step of "describing a task-level network of behaviors, which

characterizes an embedded system." This amendment is supported in the originally filed specification in at least paragraph 12.

In addition, the Office Action states that it is not clearly understood what is meant by "each of the task-level network behaviors being related through control and data flow." The present specification describes in at least paragraph 12 that high-level programming languages can be used to code an intuitive network of tasks that are related through control and data flow connections. Compilers directly map these task-level network behaviors onto a multiple processor and distributed memory hardware architecture. The Applicants submit that one skilled in the art will appreciate that task-level network behaviors can be related through control and data flow.

In addition, the Office Action states that it is not clearly understood how the step of "allocating the plurality of tasks and data to at least one of the multiple processor and to at least one of distributed memory, respectively, is preformed in claim 1. Claim 1 has been amended to recite the step of allocating the plurality of tasks to at least one processor and allocating the plurality of data to at least one distributed memory in the configurable multiple processor, distributed memory hardware architecture in response to the predicted schedule of tasks. The Applicant submits that in light of the specification this step is clearly understandable to one skilled in the art. For example, the present specification describes that in one embodiment, the allocation of the plurality of tasks and data includes an iterative allocation process that uses a demand-driven and constraint-based objective function to determine the allocation. Also, the present specification describes that, in one embodiment, the allocation of the plurality of data to the distributed memories includes allocating data to shared memories. In addition, the present specification describes that the allocation of the plurality of data to the distributed memories includes allocating data to private memories. See, for example, paragraph 16 of the present specification.

Also, the Office Action states that the term "using a demand-driven and constraint-base" in claim 6 is not clearly understood. The terms "constraint-based" and "constraint-oriented" means that the program includes certain constraints that are required by the program prior to compilation. For example, a user may require that a specific piece of data

be available to a specific memory at a specific address. The compiler is said to be constrained by this information, because the user specified this requirement in the program. The scheduling determined during compilation respects constraints of tasks requiring specific hardware resources, such as special purpose processors. The scheduling determined during compilation also respects user constraints on the placement of data and/or tasks. See, for example, paragraph 54 of the present specification. The Applicant submits that in light of the specification, the terms "constraint-based" and "constraint-oriented" are understandable to one skilled in the art.

The term "demand-driven" refers to the objective that the allocation algorithm utilizes for the scheduling. As each node is allocated, a demand is placed on each subsequently allocated node because the cost associated with each subsequent node increases. Thus, the cost associated with each node is encapsulated in a demand function. See, for example, paragraph 55 of the present specification. The Applicant submits that in light of the specification, the term "demand-driven" is understandable to one skilled in the art.

Also, the Office Action states that the term "a demand function" in claim 23 is not clearly understood. A demand function is calculated based at least in part on a constraint related to at least one of a plurality of tasks in the schedule of tasks. For example, the demand function can be calculated based at least in part on the task-level network of behaviors. The demand function can also be calculated based at least in part on an impact on the schedule of tasks. In addition, the demand function can also be calculated based at least in part on an impact on data movement. In one embodiment, the demand function is calculated based at least in part on prior allocation decisions. See, for example, paragraph 21 of the present specification. The Applicant submits that in light of the specification, the term "demand-function" is understandable to one skilled in the art.

Also, the Office Action states that it is uncertain how the step of "defined as the least negative impact on at least one performance factor" in claim 29 is performed. An example of least negative impact is presented in paragraph 63 of the present specification. In this example, the task with the highest demand is allocated to a processor with the least cost. The term "cost" is defined as the least negative impact on performance factors, such as schedule

and data movement. An example of a metric for cost is a weighted sum of the impact on the schedule and the impact on data movement. The Applicant submits that in light of the specification, the term "defined as the least negative impact on at least one performance factor" is understandable to one skilled in the art.

Rejections under 35 U.S.C. §103(a)

Claims 1-14 and 23-36 are rejected under 35 U.S.C. §103(a) as being unpatentable over WO Patent No. 0060460 to Mattioli (hereinafter "Mattioli"). To be unpatentable under 35 U.S.C. §103(a), the differences between the subject matter sought to be patented and the prior art must be such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the reference teachings. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.

Independent Claim 1 and Dependent Claims 1-14

The Office Action states that Mattioli teaches the invention substantially as claimed including a method of mapping a plurality of tasks and data onto a multiple processor, distributed memory hardware architecture. The Office Action further states that Mattioli did not specifically teach task-level network behaviors. The Office Action then concludes that it would have been obvious to one of an ordinary skill in the art at the time the invention was made to have recognized that a plurality of operations is functionally equivalent to task-level network behaviors, represented by high-level language to allow the designer to determine the mapping.

Independent claim 1 has been amended to recite the step of describing a task-level network of behaviors, which characterizes an embedded system, onto a multiple processor and distributed memory hardware architecture. The present invention relates to methods and apparatus for mapping a high-level language description of an embedded system into a configurable hardware architecture of a custom integrated circuit. The task-level network of

behaviors recited in amended independent claim 1 describes an embedded system. A high-level programming language is used to allow the designer to code a network of tasks, which describe an embedded system. The compiler is used to directly map a task-level network of behaviors that describes an embedded system onto a configurable multiple processor and distributed memory hardware architecture. See, for example, paragraphs 12 and 35.

In contrast, Mattioli describes mapping signal processing applications onto parallel computers. See Mattioli lines 1-7. Mattioli states that the object of his invention is a generic process for assisting the mapping of systematic signal processing applications onto a computer with homogeneous parallel architecture. See Mattioli page 3, lines 13-16. The Applicants submit that the methods described in Mattioli are fundamentally different from the method claimed in amended independent claim 1. In particular, the methods described in Mattioli map particular signal processing applications and not a task-level network of behaviors that describes an embedded system as claimed in amended claim.

The Office Action states that Mattioli did not specifically teach task-level network behaviors, however, Mattioli does disclose a plurality of operations on page 4, lines 12-15. The description in Mattioli on page 4, lines 12-15 teaches how systematic signal processing application are formed from sequences of tasks which are to be expressed by loop nets which are well-structured and parallel. The Applicants submit that the description on Mattioli page 4, lines 12-15 does not each or suggest the task-level network of behaviors that describe an embedded system as claimed in amended claim 1.

The task-level network of behaviors that describes an embedded system as claimed in amended claim 1 is not equivalent to the sequence of tasks that are described Mattioli. The description on Mattioli page 4, lines 12-15 is a description of a sequence of software tasks that are performed on a computer with a fixed homogeneous parallel architecture. See Mattioli, for example, page 3, lines 13-16 and page 8, lines 10-21. Thus, the sequence of software tasks described in Mattioli does not describe an embedded system. Rather, the sequence of software tasks is performed on a computer with a fixed architecture.

In addition, independent claim 1 has been amended to recite a method of mapping a plurality of tasks and mapping a plurality of data onto a configurable multiple processor,

distributed memory hardware architecture. This amendment is supported by the present specification. See, for example, the description of FIG. 3 paragraphs 41-43. Mattioli does not teach or suggest mapping a plurality of tasks and mapping a plurality of data to a configurable multiple processor. In contrast, Mattioli describes a process for mapping signal processing applications onto a computer with fixed homogeneous parallel architecture in which all the processors are identical. All the processors execute the same instruction or the same sequence of instructions. The routing of the data between the different processors is static, that is, the data paths between the processors are dictated before initialization of each mode. See, for example, Mattioli, page 8, lines 10-21.

In view of the above remarks, the Applicant respectfully submits that a *prima facie* argument for obviousness has not been made because all the claim limitations are not taught or suggested by Mattioli and the other prior art of record. Therefore, the Applicant submits that independent claim 1 as currently amended is not unpatentable over Mattioli. The Applicant also submits that dependent claims 2-14 are allowable as depending from an allowable base claim.

Independent Claim 23 and Dependent Claims 24-33

The Office Action states that Mattioli does not specifically teach the claimed task-level network behaviors, but does disclose plurality operations. The Office Action concludes by stating that it would have been obvious to one of an ordinary skill in the art to have recognized that the plurality of operations is functionally equivalent to the claimed task-level network behaviors.

Independent claim 23 has been amended to recite that the task-level network of behaviors characterizes an embedded system. As described in connection with the rejection of claim 1, the methods described in Mattioli map particular signal processing applications and not a task-level network of behaviors that describe an embedded system as claimed in amended independent claim 23. The task-level network of behaviors claimed in claim 23, as currently amended, is not equivalent to the sequence of tasks that are described Mattioli because the sequence of software tasks described in Mattioli does not describe an embedded system. Rather, the sequence of software tasks described in Mattioli is performed on a computer with a fixed architecture.

In addition, independent claim 23 has been amended to recite a method for executing a schedule of tasks in a configurable multiple processor, distributed memory architecture. This amendment is supported by the present specification. See, for example, the description of FIG. 3 paragraphs 41-43. Mattioli does not teach or suggest a method for executing a schedule of tasks in a configurable multiple processor. In contrast, as described in connection with the rejection of independent claim 1, Mattioli describes a process for mapping signal processing applications onto a computer with fixed homogeneous parallel architecture in which all the processors are identical.

In view of the above remarks, the Applicant respectfully submits that a *prima facie* argument for obviousness has not been made because all the claim limitations are not taught or suggested by Mattioli and the other prior art of record. Therefore, the Applicant submits that independent claim 23 as currently amended is not unpatentable over Mattioli. The Applicant also submits that dependent claims 24-33 are allowable as depending from an allowable base claim.

Independent Claim 34 and Dependent Claims 35-36

The Office Action states that independent claim 34 is a system claim that corresponds to the method of independent claim 1. Independent claim 34 has been amended to recite a means for describing a task-level network of behaviors, which characterizes an embedded system. As described in connection with the rejections of claims 1 and 23, the methods described in Mattioli map particular signal processing applications and not a task-level network of behaviors that describe an embedded system as claimed in independent claim 34 as currently amended. The task-level network of behaviors that characterizes an embedded system claimed in amended independent claim 34 is not equivalent to the sequence of tasks that are described in Mattioli because the sequence of software tasks described in Mattioli does not describe an embedded system. Rather, the sequence of software tasks described in Mattioli is performed on a computer with a fixed architecture.

In addition, independent claim 34 has been amended to recite a compiler for mapping a plurality of tasks and data onto a configurable multiple processor, distributed memory architecture. This amendment is supported by the present specification. See, for example,

the description of FIG. 3 paragraphs 41-43. Mattioli does not teach or suggest mapping a plurality of tasks and data onto a configurable multiple processor. In contrast, as described in connection with the rejections of independent claims 1 and 23, Mattioli describes a process for mapping signal processing applications onto a computer with fixed homogeneous parallel architecture in which all the processors are identical.

In view of the above remarks, the Applicant respectfully submits that a *prima facie* argument for obviousness has not been made because all the claim limitations are not taught or suggested by Mattioli and the other prior art of record. Therefore, the Applicant submits that independent claim 34 as currently amended is not unpatentable over Mattioli. The Applicant also submits that dependent claims 35-36 are allowable as depending from an allowable base claim.

CONCLUSION

Claims 1-14 and 23-36 are pending in the present application. Claims 1, 3-6, 13-14, 23, 29, and 34-36 have been amended. The Applicant respectfully requests reconsideration of the pending claims in light of the amendments and arguments presented in this Amendment and Response.

If, in the Examiner's opinion, a telephonic interview would expedite prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,

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